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IBIS Data for CML,PECL and LVDS Interface Circuits

MAXIM High-Frequency/Fiber Communications Group

MAXIM

Maxim Integrated Products

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1 Introduction

The integrated circuits found in optical modules and system back-planes rely on the high frequency performance of interconnections. These high-speed circuits need to be modeled to verify signal integrity with imperfect connectors and transmission lines. Model information for select Maxim fiber integrated circuits (ICs) is made available in IBIS data format at http://www.maxim-ic.com/ibis.cfm. Interpretation and limitations of IBIS data in fiber circuit interfaces are described in this paper.

IBIS (I/O Buffer Information Specification) is a data file containing necessary information for modeling step response and termination impedance of an IC. Signal integrity analysis software uses IBIS data to investigate issues such as reflection, cross-talk and EMI as illustrated in Figure 1.

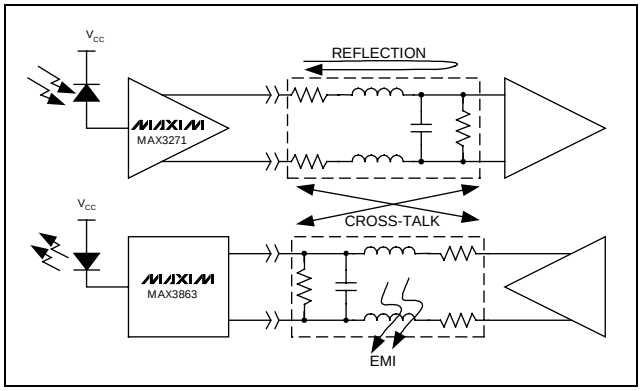

Figure 1. Fiber Module Signal Integrity

Block diagrams for the elements of an IBIS data file are shown in Figure 2a and Figure 2b. Active circuit elements are characterized in IBIS as voltage-controlled current sources. Current source information is provided in tables of V-I data for each active state of the buffer. IBIS files are not models but simply data. Users of IBIS must pay attention to how the IBIS data relates to the device being modeled, and verify that the results are reasonable. A complete specification for the most current version of IBIS can be obtained from; http://www.eigroup.org/ibis/specs.htm

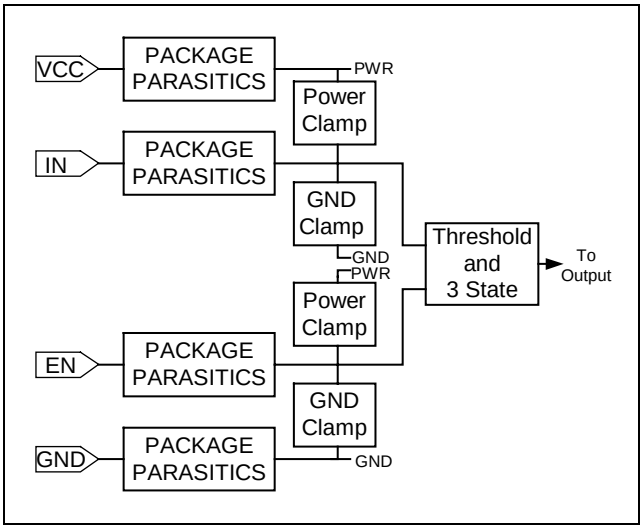

Figure 2a. Input Schematic of IBIS Data Blocks

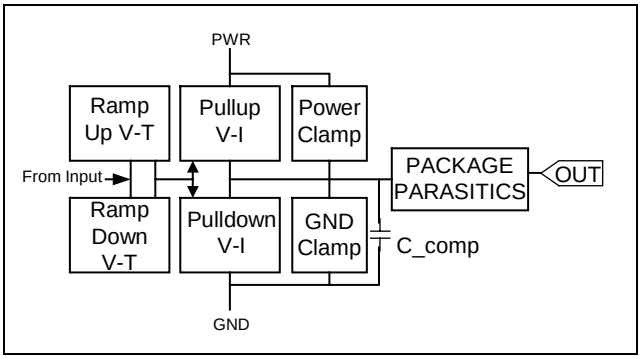

Figure 2b. Output Schematic of IBIS Data Blocks

Transition between states is described by voltage vs. time (V-T) data. Transitions occur when voltage at the device input exceeds the specified threshold voltage Vinh or Vinl. During transient conditions the weighting of the output V-I sources may be determined using the V-T data to scale the V-I current by a factor K(t) as shown in Figure 3. IBIS simulators may compute K(t) automatically. This computation is described in a paper by Tehrani, Chen and Fang; "Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS."[1]

[1] Department of Electrical Engineering State University of New York at Binghamton. http://www.sigrity.com/papers/ectc96/ectc96ibis.pdf

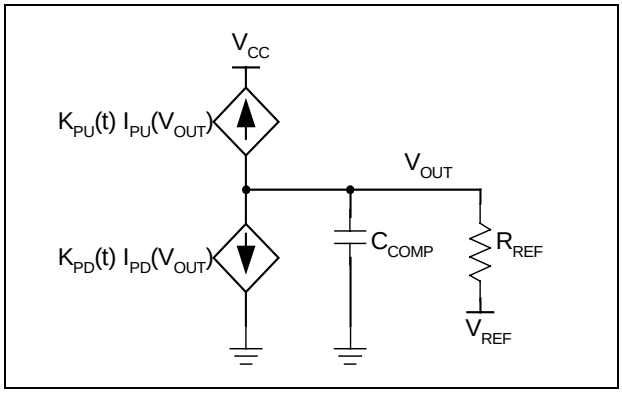

Figure 3. Transient State IBIS Data Utilization

Other types of fiber interface models are also available. Input and output (I/O) models in SPICE (Simulation Program for Integrated Circuit Emulation) allow more detailed analysis of the IC interface. Information on some SPICE models may be requested from Maxim Fiber and HF Communications.

2 Devices Modeled by IBIS

High speed IC electrical interfaces generally are of the following types CML, PECL or LVDS.

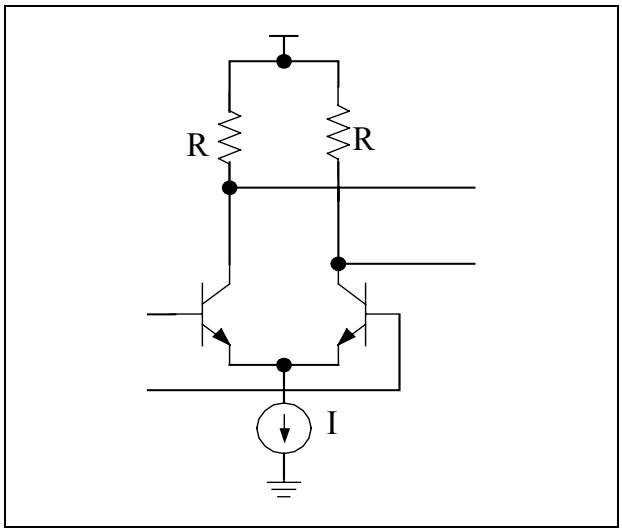

Figure 4. CML Output

The CML output is the simplest interface, being just a current source switched between resistors. Output voltage change for a new state is then I·R.

A voltage follower added to the differential pair, models a PECL output. The PECL output is more of a constant voltage source as the impedance seen looking into the output is reduced by the Beta of the voltage follower transistor.

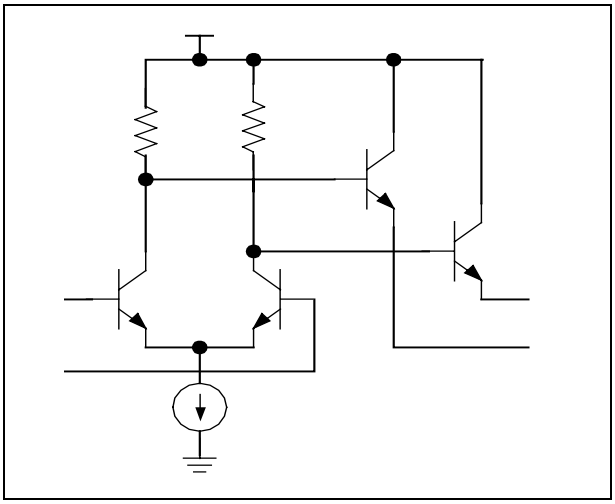

Figure 5. PECL Output

The voltage source of the PECL output can be modified to maintain the output impedance at 50Ω and the output common voltage near 1.2V. This is done in LVDS by adding a current source and resistor in each emitter circuit of the voltage follower. The emitter current is then adjusted so that the impedance seen looking into the output will be 50Ω. A feedback loop senses the common mode voltage and controls it to be near a reference voltage.

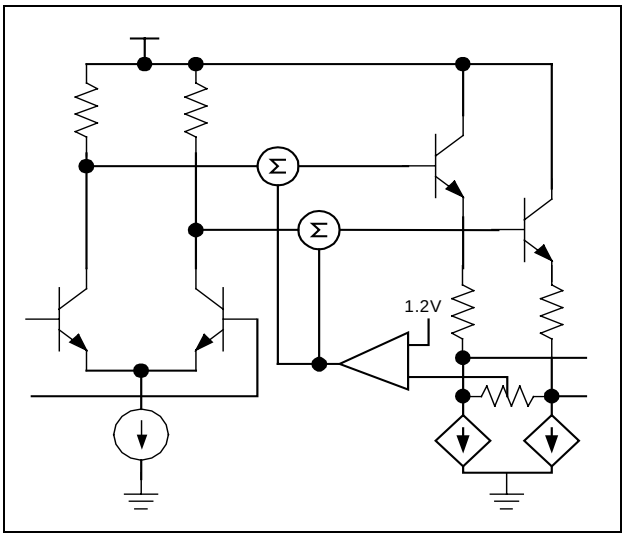

Figure 6. LVDS Output

3 V-I Data for IBIS

The V-I curve for the active element of the CML output represents the transistor current source in its conducting state. Only one V-I curve is needed for this sink type of output. The pullup resistor is customarily included in the V-I curve for the ESD diodes as shown in Figures 8 and 9.

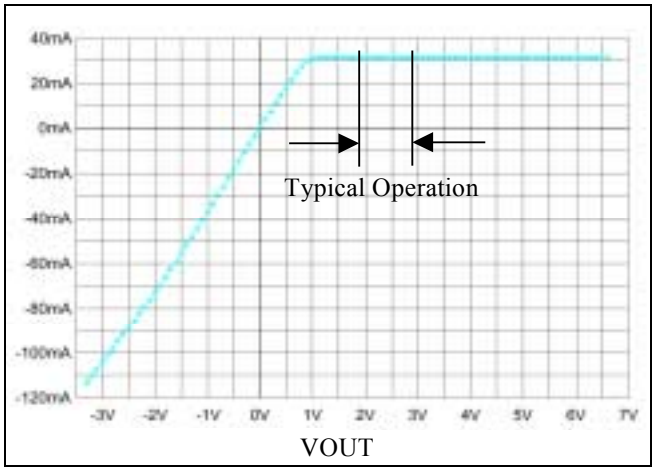

Figure 7. CML Output Pulldown V-I

Currents are provided for voltages from –VCC to 2VCC per IBIS recommendation. Designs using CML outputs will have a much smaller output voltage range than this as shown in Figure 7. Minimum CML output voltage should never approach the knee of the V-I curve where current compliance no longer holds. Maximum voltage should never exceed VCC+0.5V in normal operation. Check simulation results of Absolute Maximum Ratings as listed in the data sheet, to assure that the part is being used correctly.

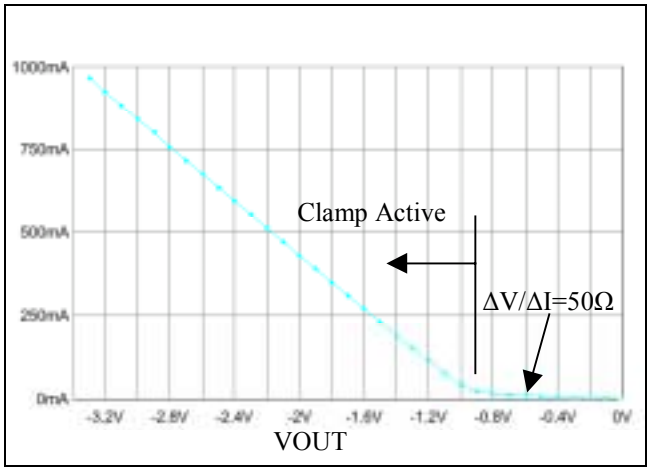

Figure 8. Power Clamp Curve with 50 Ω Pull-up

The pullup and pulldown sources are turned on and off by the weighting factor K(t) so that currents are recorded for all voltages. Voltages in the clamp diode curves don't overlap as both voltage-controlled current sources, representing the clamp diodes, are to be connected to the model at all times.

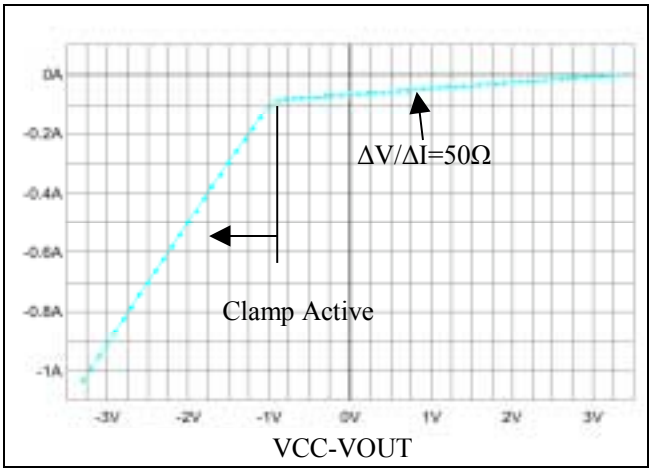

Figure 9. Ground Clamp Curve with 50 Ω Pull-up

For PECL outputs the clamp curves are similar to CML, but without the slope in the non-conducting state of the ESD diode. The V-I curves are much different however, due to lower output impedance.

The voltage-controlled current sources for PECL are VCC referenced in both states as shown in Figure 10. The V-I curves representing the PECL voltage source are shown in each VCC-referenced state in Figure 11 and Figure 12.

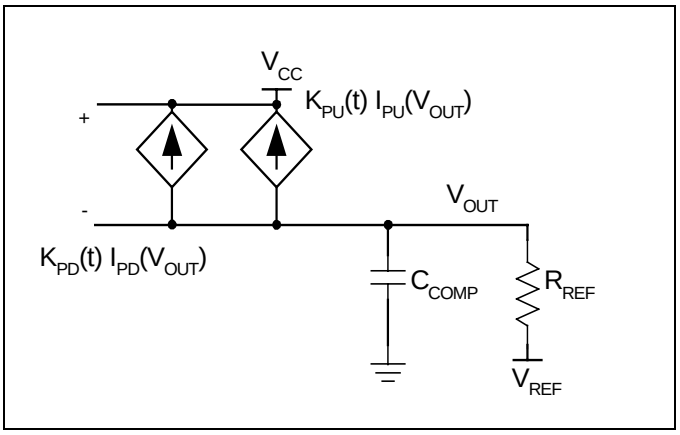

Figure 10. IBIS Data Utilization for PECL Outputs

When the PECL outputs are properly terminated to VCC-2V through 50Ω the output voltage should be near VCC-1V for logic high and VCC-1.7V for logic low. This is the low impedance portion of the V-I curve. Voltages significantly different from these indicate misapplication of the part.

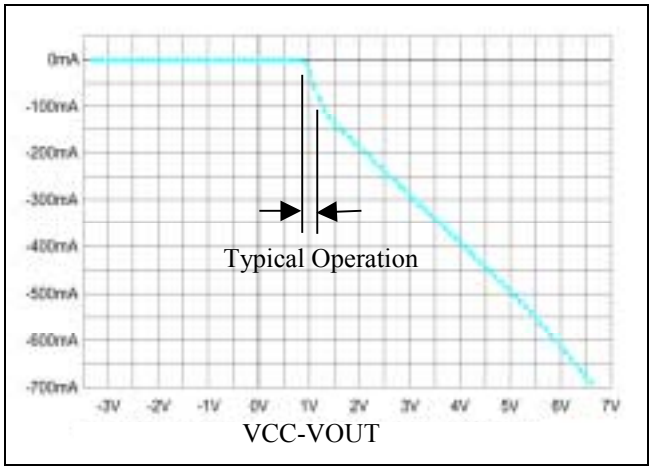

Figure 11. PECL Output V-I, High State

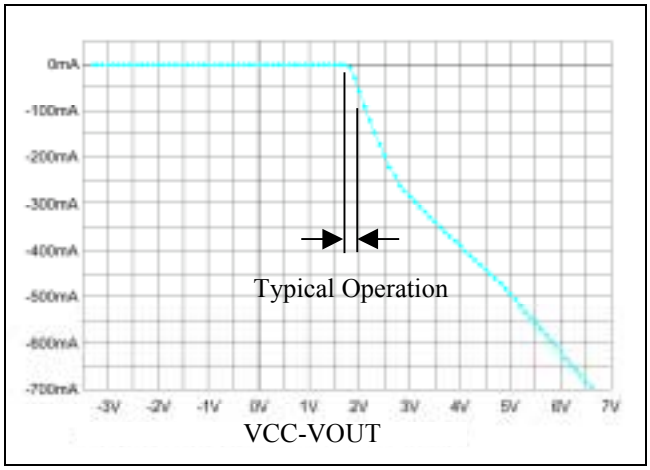

Figure 12. PECL Output V-I, Low State

It is also possible to include the V-I data for the clamp diodes with the data for the pullup and pulldown V-I curves. In this case both diodes are included in the data for each state of the device. Of course only one of the pullup or pulldown data sets is active in a steady state.

The LVDS V-I data in the high state is referenced to VCC while the low state is referenced to ground. This corresponds to the standard IBIS data utilization shown in Figure 3. Normal operation of the LVDS Output will be at voltage swings from 1.0V to 1.4V with respect to ground. The back termination impedance in this region is 50Ω as can be seen in Figures 13 and 14. If simulation results show voltages outside this range the part is being misapplied.

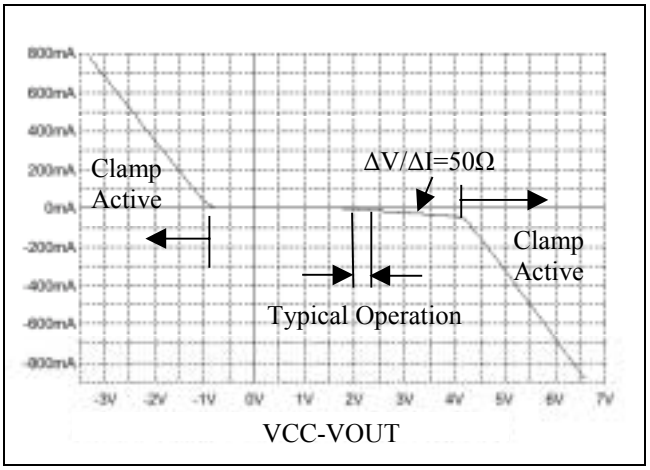

Figure 13. LVDS Output V-I, High State with Clamp Diodes

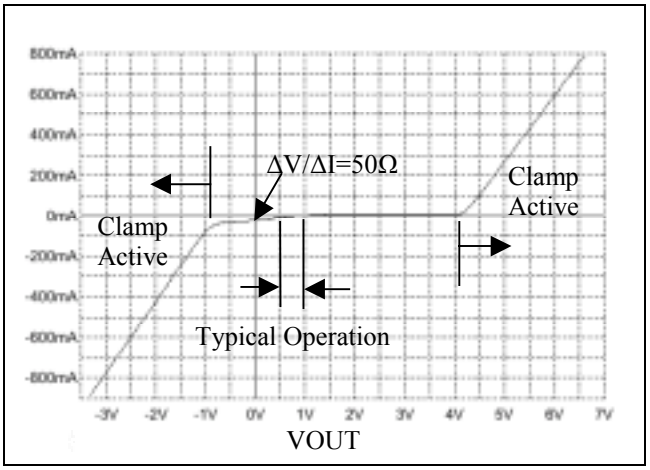

Figure 14. LVDS Output V-I, Low State with Clamp Diodes

An interesting feature for extracting IBIS data for LVDS outputs is the feedback loop that controls the common-mode voltage. If a voltage is forced on the output it opens the feedback loop. Without feedback, the gain of the error amplifier (shown in Figure 6) will drive the outputs to one rail or the other. The output should not be forced to a voltage in actual applications.

4 V-T Data for IBIS

4.1 Golden Waveforms

The V-T data provides a golden waveform showing how the IC should respond to a known load. Simulators use this data to extract weighting factors ($K_{PU}(t)$, $K_{PD}(t)$) to control the voltage-controlled current sources described by the V-I data. This prevents problems when V-I data contains

discontinuities like those seen for PECL outputs in Figure 11.

Adequate waveforms may be produced using the IBIS file dV/dt data only. Quick modifications of the model are possible because only a pair of data entries is modified to change the rise time. This simple scheme can produce reasonable waveforms for CML outputs. The output voltage for CML will have the same shape as the ramp given to the current. This is not the case for PECL outputs. The sharp discontinuities in the V-I curves produce very strange waveforms if the pullup and pulldown current weighting factors shown in Figure 12 are not carefully extracted.

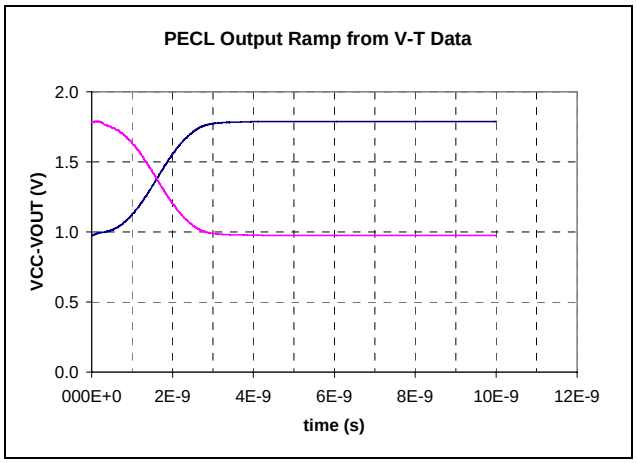

Figure 15. PECL Ramp Using V-T Data

The simulation result for a PECL output using V-T data is shown in Figure 15. The same simulation was repeated with only dV/dt data with results shown in Figure 16. Clearly the dV/dt data is not satisfactory for simulating PECL rise/fall times.

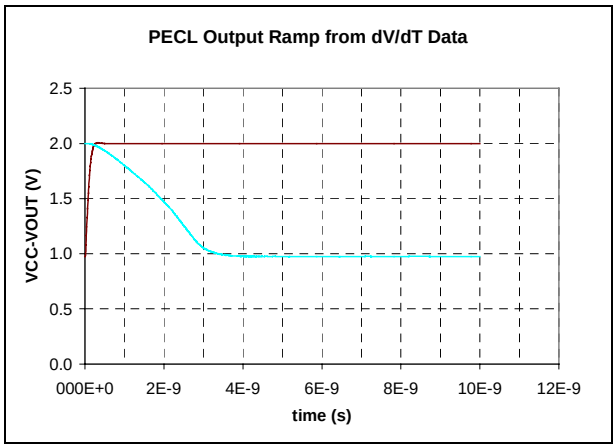

Figure 16. PECL Ramp Using dV/dt Data

4.2 V-T Data Extraction

The IBIS specification recommends that the V-T data be extracted with no package parasitics. When V-T data is derived from simulation, the parameters R_dut, L_dut and C_dut will not be used, indicating V-T is for the die only. Since R_dut, L_dut and C_dut correspond to R_pkg, L_pkg and C_pkg, care must be taken not to incorporate both sets of parameters in the simulation. To do so would double count the package parasitic.

The interface types described here all have one rising and one falling V-T data set. This matches the IBIS standard of 2 V-T curves for each active device. Even though LVDS outputs would appear to have 2 active output devices the second device is a constant current sink so the output characteristics are always due to the emitter follower.

4.3 V-T Data Limitations

IBIS data cannot model deterministic jitter (DJ). This limitation is because the V-T data always has the same logic zero and logic one voltage for any transition. These voltages are independent of the duration of the previous state.

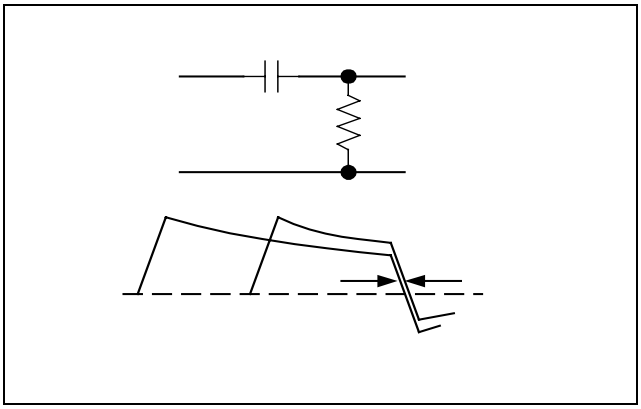

Figure 17. Simple Example of Deterministic Jitter

A simple example of DJ would be the sag caused by a DC block shown in Figure 17. If the capacitor is too small, a significant change in voltage may take place before the next transition, resulting in a shift in time of the transition relative to a clock. IBIS does not model the DJ from the incomplete transition during the previous state of the IC. An extreme example would be PECL outputs loaded by too much capacitance. The transistor Beta rolls off with increasing frequency causing the capacitance in the

emitter circuit to appear from the base as a negative resistance. **Excess capacitance on PECL outputs may cause oscillations**. Models based on IBIS cannot predict this, therefore be careful.

Latency specifications are given for a few Maxim fiber parts, such as the MAX3640 cross-point switch and the MAX3784 equalizer. The V-T IBIS data can be a means of tracking the delay through the part. Fiber parts with specified latency are built with evaluation boards to allow verification of the specification. The V-T data for such parts can be reliable for predicting latency. When no specification for latency is provided the IBIS data may not be accurate for determining the delay through the part.

5 Differential Inputs in IBIS

Differential I/O signals can have different impedance, depending on how the signal pair is driven. In most applications the driving signals swing in opposite directions about a common mode voltage V_{CM} as shown in Figure 18.

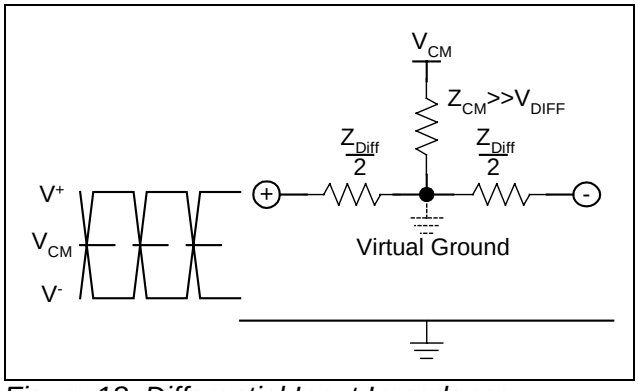

Figure 18. Differential Input Impedance

Differential drive forms a virtual ground at the center of the impedance connecting the inputs. The impedance seen by one of the differential signals is then Z_{Diff}. If the signal pair is driven together (referred to as common mode) then the impedance seen is the common mode impedance ~Z_{CM}.

Current versions of IBIS keep track of pins that form differential pairs. A simple way to model the value of Z_{Diff} is through the use of the IBIS model type, [R Series] as shown in Figure 19a. No provision was made in the original version of IBIS for differential signals. Not all simulators support the [R Series] model. Correct input termination should be verified with the IBIS data users simulator.

Other differential input modeling methods include assuming the input signals are always differential, so that the virtual ground in Figure 18 is always present. The inputs are then de-coupled and the impedance Z_{Diff} /2 can be included in the V-I curve of the input ESD diodes as shown in Figure 19b. This method will not respond correctly if the input signals lose their symmetry.

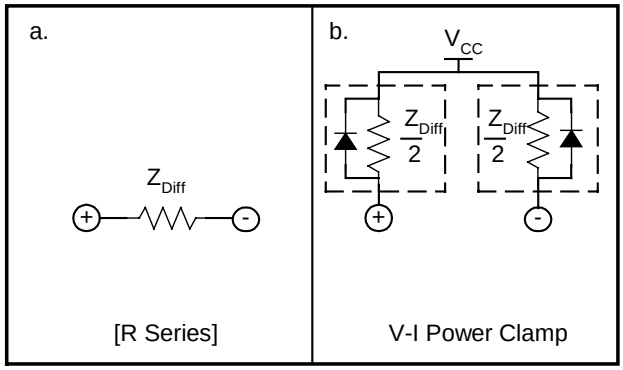

Figure 19. Differential Input IBIS Representations

6 Simulation Checklist

1. Make sure input and output voltages do not exceed the absolute maximum specified for the part in the data sheet.

2. Normal output voltage ranges for fiber interfaces should be near the values shown in Table 1.

Table 1 Typical Operating Voltages

Family	Logic High	Logic Low
CML	VCC	VCC-0.4V to VCC-1.6V
PECL	VCC-1V	VCC-1.7V
LVDS	1.4V	1.0V

3. Verify that rise and fall times agree with the data sheet and the V-T data provided with the IBIS model. Changes in rise time may be due to a change in load conditions, but might be caused by double counting the package parasitics or failure to utilize the V-T data in the simulation.

4. Limit capacitance loading on PECL outputs. When in doubt a SPICE model of the output should be tested for stability.

5. Simulations using IBIS data may predict deterministic jitter added by the circuit interconnect. Actual DJ of the part modeled may not be seen in the IBIS simulation.

6. Do not assume that the latency described by the V-T data is correct. If a part does not have a specified latency the simulation data cannot be relied on for the correct delay through the part.

7. For differential inputs modeled by a series resistor [R Series], as in Figure 19a, check that the simulator accepts this model.

1. For differential inputs, modeled with 50Ω resistors to AC ground (virtual ground), make sure the loading on both inputs is well balanced. Correct simulation relies on the input voltages being equal and opposite about the DC common mode voltage at the AC ground. See Figure 19b.

7 Conclusion

Signal Integrity analysis based on IBIS data is possible for interface ICs. The three common interfaces are CML, PECL and LVDS. Analysis with IBIS of the fiber IC will produce correct output voltages, similar to Table 1, with typical loads. Verification of the transitions can be made based on the specified rise and fall times as well as by using the V-T data provided in the IBIS data file.

Analysis beyond what IBIS can handle may be needed in extreme cases. As an example, a PECL output driving a capacitor may need to be analyzed with SPICE. Also, unbalanced differential input signals can be a problem depending on the simulator used.